 



**Optimized Chip-on-Wafer Heterogeneous Integration**: Sony researchers will discuss an advanced process for fine-pitch face-to-back (F2B) chip-on-wafer (CoW) integration in 3D heterogeneous integrated systems. It features a novel chemical mechanical polishing (CMP) process that incorporates oxidation inhibitors to optimize Cu recess control for enhanced fine-pitch Cu–Cu hybrid bonding. They successfully implemented the optimized process on a single chip for various pad sizes (from 3.0 µm to 1.0 µm), achieved void-free bonding, and saw a significant improvement in Kelvin connection yields (i.e., low-resistance connections) versus conventional processing. Moreover, excellent electromigration resistance was observed, with projected device lifetimes exceeding 10 years. The researchers say these results validate the effectiveness of the proposed fabrication process for high-density three-layer stacked chip-on-wafer-on-wafer (CoWoW) structures, such as stacked back-illuminated CMOS image sensors (BI-CIS).

* **Top left image**: The evolution and future prospects of stacked back-illuminated CMOS image sensors (BI-CIS).
* **Top right image**: Schematic diagram of a 3-layer vertically stacked structure (CoWoW). The middle and bottom wafers are connected via face-to-face (F2F) WoW. The top chip is placed face-down on the backside Cu pads of the middle wafer.
* **Lower image**: Cross-sectional SEM images of daisy chains for (a) 3.0-µm pad/6.0-µm pitch, (b) 1.4-µm pad/2.8-µm pitch, and (c) 1.0-µm pad/2.0-µm pitch.

**(IP session #39, “*Advanced Face-To-Back CoW 2.0-µm pitch Cu–Cu Hybrid Bonding Process for Three Layer-Stacked 3D Heterogeneous Integration*,” A. Urata et al, Sony)**